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Characterization of 6H-SiC JFET Integrated Circuits Over A Broad Temperature Range from -150 °C to +500 °C

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Abstract: The NASA Glenn Research Center has previously reported prolonged stable operation of simple prototype 6H-SiC JFET integrated circuits (logic gates and amplifier stages) for thousands of hours at +500 °C. This paper experimentally investigates the ability of these 6H-SiC JFET devices and integrated circuits to also function at cold temperatures expected to arise in some envisioned applications. Prototype logic gate ICs experimentally demonstrated good functionality down to -125 °C without changing circuit input voltages. Cascaded operation of gates at cold temperatures was verified by externally wiring gates together to form a 3-stage ring oscillator. While logic gate output voltages exhibited little change across the broad temperature range from -125 °C to +500 °C, the change in operating frequency and power consumption of these non-optimized logic gates as a function of temperature was much larger and tracked JFET channel conduction properties.

Introduction

NASA is developing very high temperature semiconductor integrated circuits (ICs) based on silicon carbide (SiC) junction field effect transistors (JFETs) for beneficial use in the hot sections of aircraft engines and for future Venus surface exploration missions. Additional applications for electronics that can operate at temperatures greater than 300 °C include automotive engines and deep-well drilling [1]. The fabrication of 6H-SiC JFETs, IC formation using single-level metal interconnect, and subsequent *operation of transistors and simple circuits for thousands of hours at 500 °C* have been previously reported [2-5]. In addition to extreme high temperature operating capability, some applications may require functionality at cold temperatures well below freezing, as might occur during engine cold-starts and deep-space transits. This paper reports initial measurements of the electrical characteristics of these 6H-SiC JFET devices and ICs at very cold temperatures down to -150 °C where ICs were no longer functional.

Experimental Procedures and Results

Experimental procedures (including JFET cross-section) for chip fabrication and electrical measurements have largely been described previously [2-6]. Some chips were custom packaged for high temperature by a commercial vendor [7], while others were packaged at NASA [8]. Fig. 1 shows the schematic of a 6H-SiC digital two-input NOR logic gate IC, one of the circuits that was characterized at both cold and hot temperature extremes. Two-input NAND gates, for which input transistors J_{INA} and J_{INB} reside in series combination instead of parallel combination illustrated in Fig. 1, were also tested. Negative logic signal voltages and substrate bias ($V_{SUB} = -V_{SS}$) were employed to keep JFET pn junctions reverse biased. Aside from high temperature

durability/stability, absolutely no effort was made to optimize speed, power, or other performance metrics of these first-generation prototype ICs based on 10μm gate length dimensions. NOR gates were packaged with access to internal nodes so that the temperature-dependent characteristics of the transistors and resistors could be separately measured in addition to the overall logic gate input/output characteristics. Testing below room temperature was carried out using a commercially available cold chamber, while a commercial box oven was used for high temperature testing.

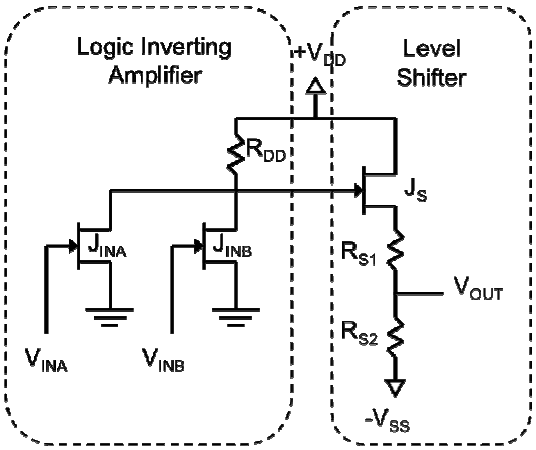

Fig. 1: Schematic of prototype 6H-SiC NOR logic gate. Resistors are implemented in the same n-layer as the JFET n-channel, which helps facilitate stable operation over a broad (-125 °C to +500 °C) temperature range.

JFETs and Resistors. Fig. 2 summarizes the measured temperature dependence of key 6H-SiC JFET and epitaxial resistor parameters from one of the characterized NOR logic gates. Saturated drain current I_{DSS} (grey diamonds, measured at drain bias V_D = 20V and gate bias V_G = 0V) and transconductance g_m (black squares) measured from the input SiC JFETs (J_{INA} in parallel with J_{INB}), as well as the resistance of R_{DD} (black circles) are plotted. Since resistors and transistors were implemented using the same 6H-SiC n-channel epilayer [2-5], the electrical behavior of these elements change nearly identically with temperature, corresponding to the temperature-dependent conduction properties of the n-channel. The maximum JFET transconductance g_m and minimum R_{DD} resistance occur near room temperature. As the density of ionized electrons in the n-channel drops with decreasing temperature (expected from freeze-out of nitrogen donors [9]), the transistor gain and current decrease at about the same rate that R_{DD} increases. This enables the circuit-crucial g_m x R_{DD} product (plotted with black triangle symbols in Fig. 2) to remain nearly constant despite nearly 3-fold change in drain current caused by carrier freeze-out at cold temperature.

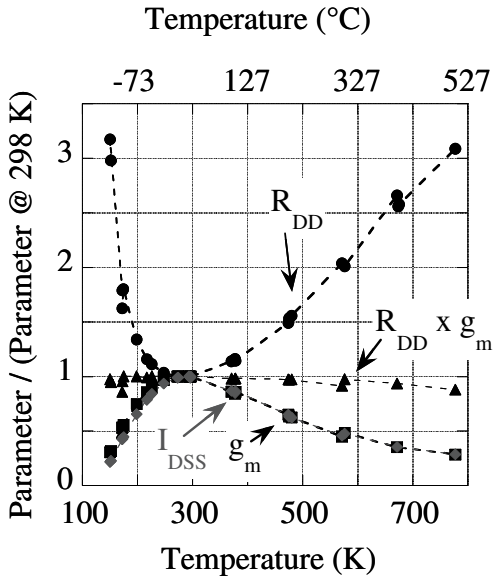

Fig. 2: Plot of measured temperature dependence of key 6H-SiC JFET and resistor parameters.

Quite similar parameter changes from degradation of channel conductivity occur as temperature is increased above room temperature to 500 °C due to thermal carrier scattering. The general trends and physics observed for the resistors and JFETs are consistent with previous SiC JFET studies [9]. It is worth noting that Fig 2 device parameters near -120 °C are quantitatively comparable to the values measured near +500 °C.

Integrated Circuits. Two-input NAND and NOR logic gate ICs experimentally demonstrated nearly temperature-independent output signal voltages from -125 °C to +500 °C. Fig. 3 compares measured operational test waveforms recorded from a packaged NAND gate at -124 °C, +20 °C, and +500 °C. Over the entire temperature range of this test, the circuit was driven by the same power supply voltages of V_{DD} = +30 V and V_{SS} = -22 V and the same high (V_{IH} = -0.5 V) and low (V_{IL} = -6.0 V) logic test input signal voltages. Despite the 624 °C temperature span, only slight

changes in the NAND gate output signal waveforms (and output high V_{OH} and output low V_{OL} voltage levels) are evident in Fig. 3. This occurs despite the large (> 3-fold) changes in temperature dependent SiC JFET and resistor parameters (Fig. 2). Under the circuit approach of Fig. 1, output voltage V_{OUT} is primarily determined by power supply voltages (fixed) and ratios of JFET/resistor parameters that stay relatively constant as a function of temperature due to their joint dependence on SiC n-channel conduction properties [6]. However, as the temperature was cooled down to -150 °C, the circuit could no longer drive a 10 MΩ oscilloscope probe to the required logic output voltages of $V_{OH} \geq V_{IH}$ and $V_{OL} \leq V_{IL}$. The NAND gate resumed functional operation upon subsequent warm-up. Similar results were measured on all logic gates (one NAND and four NORs) that have been custom-packaged and tested at low temperatures to date.

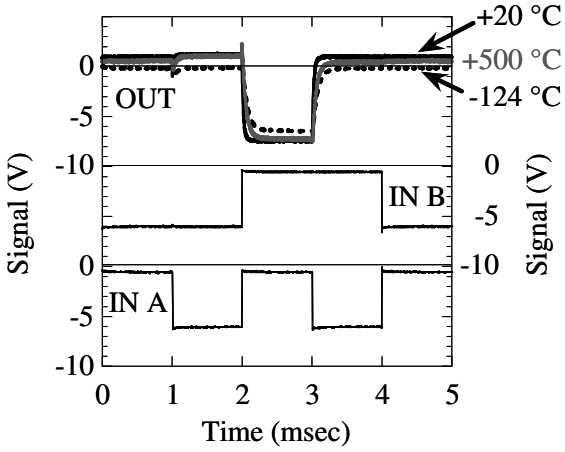

Fig. 3: Digitized waveforms recorded from experimental testing of packaged 6H-SiC NAND gate at -124 °C, +20 °C, and +500 °C with power supply voltages of V_{DD} = +30V and V_{SS} = -22 V.

While logic gate output voltages were nearly temperature independent, the power consumption and signal transition times exhibited significant dependence on temperature that tracked SiC n-channel conduction properties. As an example, Fig. 4 plots the measured power consumption of a NAND IC (black circles and squares for output low and high states, respectively) as well as the measured high-to-low logic output transition time (grey). The changes in resistor/transistor resistance/gain directly affect bias currents throughout the circuit, which in turn directly impact power dissipation and circuit node charging/discharging times. Thus, Fig. 4 circuit metrics exhibit the same temperature dependent trends seen in Fig. 2 discrete device data.

Cascaded operation of logic gates was verified by externally wiring three NOR gates (powered by V_{DD} = +26 V and V_{SS} = -26 V) residing in the cold chamber to form a ring oscillator. Even though this oscillator test was far from optimized (e.g., no output buffer, gates connected to each other and power supplies outside the test chamber via ~20 cm long unshielded wire bundles), successful operation from -125 °C to the upper temperature limit of the cold test chamber (+200 °C) was demonstrated. The measured oscillation frequency f_{OSC} peaked at room temperature at 5111 Hz. Fig. 5 summarizes the observed low and high output voltages (V_{OL} and V_{OH}) and f_{OSC} measured as a function of temperature. The benchmark drain current I_{DSS} measured from paralleled input JFETs (J_{INA} and J_{INB} of Fig. 1) of a NOR gate in the oscillator circuit is also plotted in Fig. 5 normalized to its value at room temperature. As expected, Fig. 5

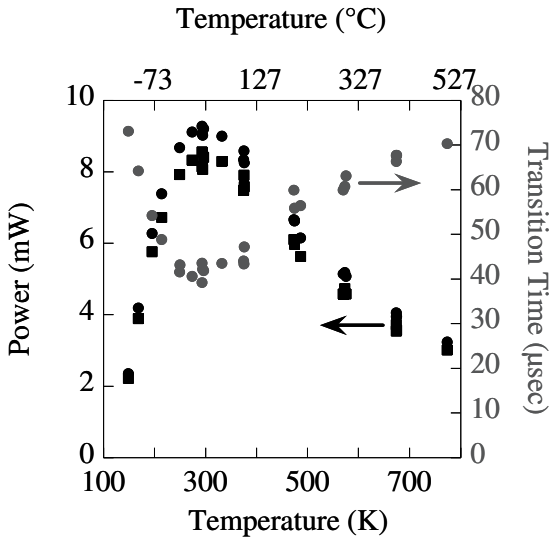

Fig. 4: NAND gate power dissipation (black symbols) and logic high to low transition times (grey circles) measured as a function of temperature. Both circuit parameters track the n-channel conduction dominated behavior of key JFET/resistor parameters seen in Fig. 2.

shows that the oscillation frequency f_{OSC} tracks JFET I_{DSS} (i.e., JFET n-channel conduction) as a function of temperature.

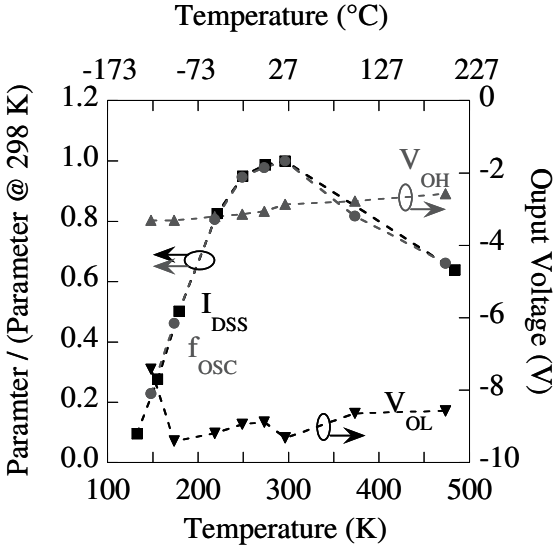

Fig. 5: Measured temperature performance of a 3-stage ring oscillator formed by externally wiring together three 6H-SiC NOR gates. High and low output levels (V_{OH} and V_{OL}) are stable, and the oscillation frequency (f_{OSC}) as a function of temperature tracks the measured I_{DSS} of the 6H-SiC JFETs.

Summary Discussion

6H-SiC JFET circuit operation changes similarly whether the temperature is raised or lowered substantially from room temperature. This is primarily due to the fact that 6H-SiC n-channel layer conductivity peaks near room temperature, dropping off at cooler temperature due to carrier freeze out and at higher temperature due to increased thermal scattering of carriers [9]. *The operational temperature range of the logic gate ICs documented in this work is to our knowledge unprecedented for a semiconductor transistor IC.*

This n-channel JFET logic family requires orders of magnitude more power than logic-equivalent gates implemented in silicon complementary metal oxide semiconductor ICs. This fact precludes extreme temperature SiC JFET ICs from reaching the very high circuit complexity and low power dissipation that is common for room temperature silicon chips. Nevertheless, shrinkage of device dimensions, power supply voltages, and other SiC JFET IC technology optimizations are expected to greatly improve power dissipation, speed, and other metrics relevant to implementing beneficially complex extreme temperature ICs. GaAs JFET IC experience suggests that SiC JFET IC circuit complexities in excess of 10^3-10^4 transistors per chip should be possible with technology optimization [10]. However, chip packaging for such an extreme temperature range, especially considering vibration and repeated thermal cycling demands of some applications, remains to be further tested.

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References

[1] P.G. Neudeck, R.S. Okojie and L.Y. Chen: Proc. IEEE Vol. 90 (2002), p. 1065.
[2] D.J. Spry, et al.: Mater. Sci. Forum Vol. 600-603 (2008), p. 1079.
[3] P.G. Neudeck et al.: IEEE Electron Device Lett. Vol. 29 (2008), p. 456.
[4] P.G. Neudeck et al.: Mater. Sci. Forum Vol. 615-617 (2009), p. 929.
[5] P.G. Neudeck et al.: Phys. Stat. Solidi A (2009), http://dx.doi.org/10.1002/pssa.200925188.
[6] M. J. Krasowski: NASA Tech Briefs Vol. 32, No. 12 (2008), p. 28.
[7] Sienna Technologies, Inc: http://www.siennatech.com/specialty.html.
[8] L.Y. Chen and J.F. Lei, in: *The MEMS Handbook, 2nd Ed.*, edited by M. Gad-el-Hak, chapter 12, CRC Press, Boca Raton FL USA (2006).
[9] F.B. McLean et al.: J. Appl. Phys. Vol. 79 (1996), p. 545.
[10] D.L. Harrington et al.: IEEE GaAs IC Symp. Tech. Dig. (1988), p. 87.